

10Gb/s XFP Optical Transceiver Module

SXP3100SV, SXP3100SV-M

(IR-2/S-64.2b, 10GBASE-ER/EW, 1550nm EML, PIN-PD)

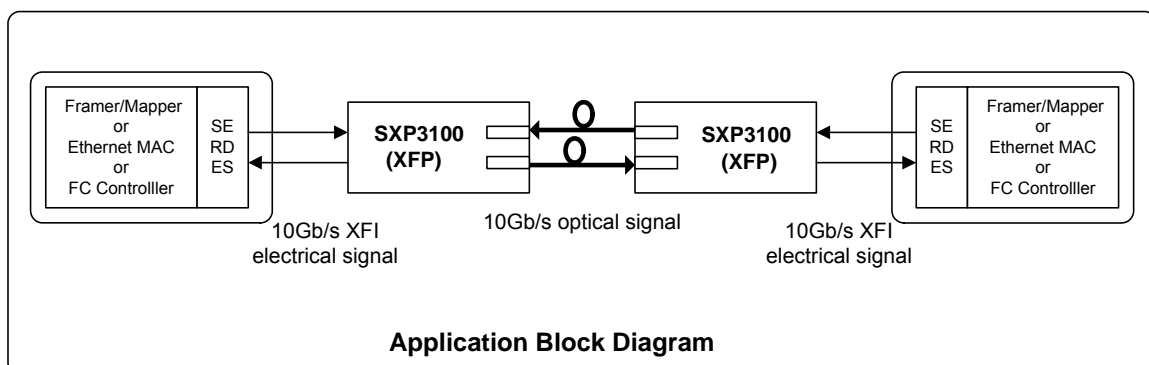
Features

- ◆ 10Gb/s Serial Optical Interface
 - ◆ High quality and reliability optical device and sub-assemblies
 - ◆ 1550nm EML laser for up to 40km over single mode fiber
 - ◆ High sensitivity PIN photodiode and TIA
- ◆ XFP MSA Revision 4.0 Compliant
 - ◆ Easy supply management for hot pluggability
 - ◆ Duplex LC Receptacle
 - ◆ XFP Mechanical Interface with color coded bail latch for easy removal (Bail color: Red)
 - ◆ XFI High Speed Electrical Interface
 - ◆ 2-wire interface for management and diagnostic monitor
 - ◆ Tx_Disable and Rx_LOS functions
- ◆ Multi-Protocol
 - ◆ SONET OC-192/SDH STM-64
 - ◆ IEEE802.3ae 10 Gigabit Ethernet
- ◆ Extended Operating Temperature range
 - ◆ Tc=-5 to 85degC (SXP3100SV-M)
- ◆ Low Power Consumption
 - ◆ +3.3V and +5.0V Power Supplies
 - ◆ Low power consumption
- ◆ RoHS6 Compliant



Applications

- ◆ SONET(OC-192)/SDH(STM64) line card
- ◆ 10GE Ethernet switches and routers
- ◆ 10GE Core-routers
- ◆ 10GE Storage
- ◆ Inter Rack Connection
- ◆ Other high speed data connections



1. General Description

The SXP3100SV-M is a very compact 10Gb/s optical transceiver module for serial optical communication applications at 10Gb/s. The SXP3100SV-M converts a 10Gb/s serial electrical data stream to 10Gb/s optical output signal and a 10Gb/s optical input signal to 10Gb/s serial electrical data streams. The high speed 10Gb/s electrical interface is fully compliant with XFI specification.

The SXP3100SV-M is designed for use in a variety of 10Gb/s SONET/SDH equipment including FEC (9.95Gb/s to 10.7Gb/s) as well as Ethernet LAN (10.3Gb/s) and WAN (9.95Gb/s) applications. The high performance cooled 1550nm EML transmitter and high sensitivity PIN receiver provide superior performance for SONET /SDH and Ethernet applications at up to 40km links.

The fully XFP compliant form factor provides hot pluggability, easy optical port upgrades and low EMI emission.

2. Functional Description

The SXP3100SV-M contains a duplex LC connector for the optical interface and a 30-pin connector for the electrical interface. Figure 2.1 shows the functional block diagram of SXP3100SV-M XFP Transceiver.

Transmitter Operation

The transceiver module receives 10Gb/s electrical data and transmits the data as an optical signal. The transmitter contains a Clock Data Recovery (CDR) circuit that reduces the jitter of received signal and reshapes the electrical signal before the electrical to optical (E-O) conversion. The optical output power is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by Tx disable signal, at TX_DIS pin. When TX_DIS is asserted High, Transmitter is turned off.

Receiver Operation

The received optical signal is converted to serial electrical data signal. The optical receiver contains a CDR circuits that reshapes and retimes an electrical signal before sending out to the XFI channel (i.e. XFP connector and high speed signal traces).

The RX_LOS signal indicates insufficient optical power for reliable signal reception at the receiver.

Management Interface

A 2-wire interface (SCL, SDA) is used for serial ID, digital diagnostics and other control /monitor functions. The address of XFP transceiver is 1010000x. MOD_DESEL signal can be used in order to support multiple XFP modules on the same 2-wire interface bus.

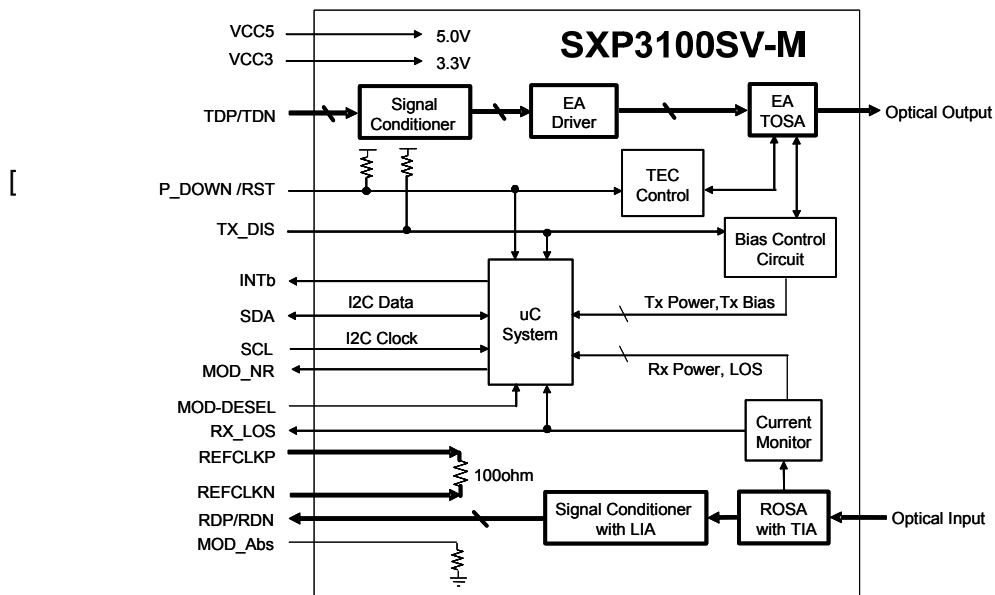
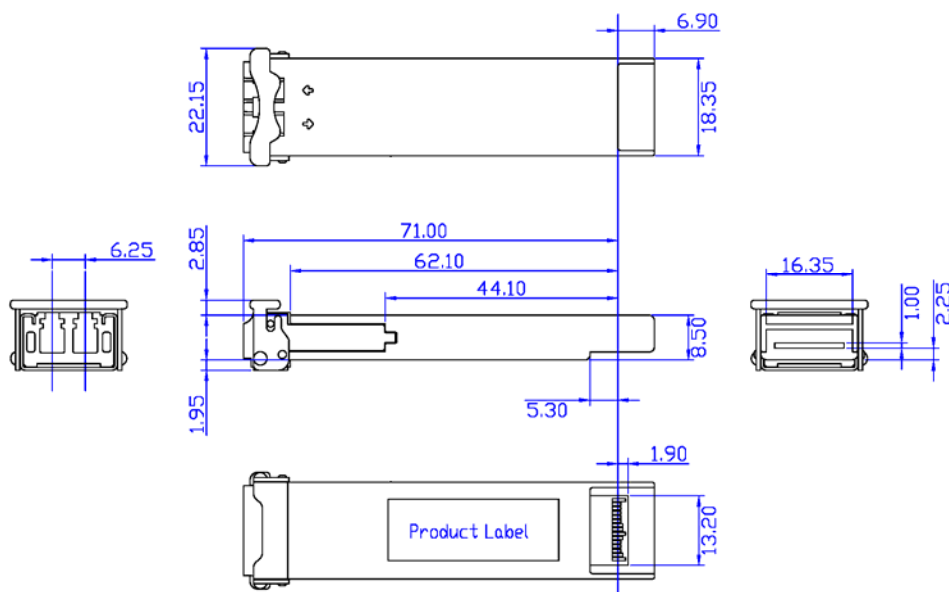


Figure 2.1. Functional Block Diagram

3. Package Dimensions

Figure 3.1 shows the package dimensions of SXP3100SV-M. SXP3100SV-M is designed to be compliant with XFP MSA specification. Package dimensions are specified in section 6.3 of the XFP MSA specification Rev. 4.0.



* Bail color is Red.

Unit : mm

Figure 3.1. Package Dimensions

4. Pin Assignment and Pin Description

4.1. XFP Transceiver Electrical Pad Layout

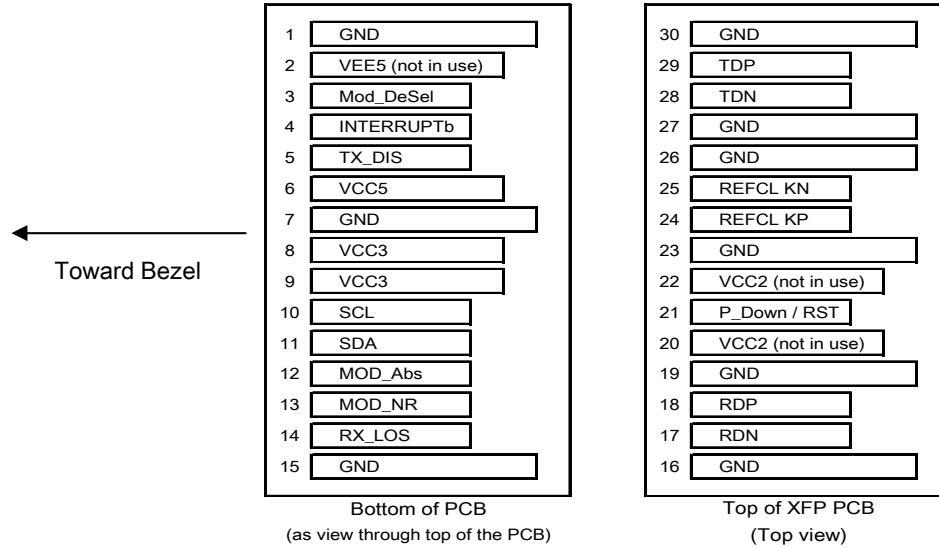


Figure 4.1. XFP Transceiver Electrical Pad Layout

4.2. Host PCB XFP Pinout

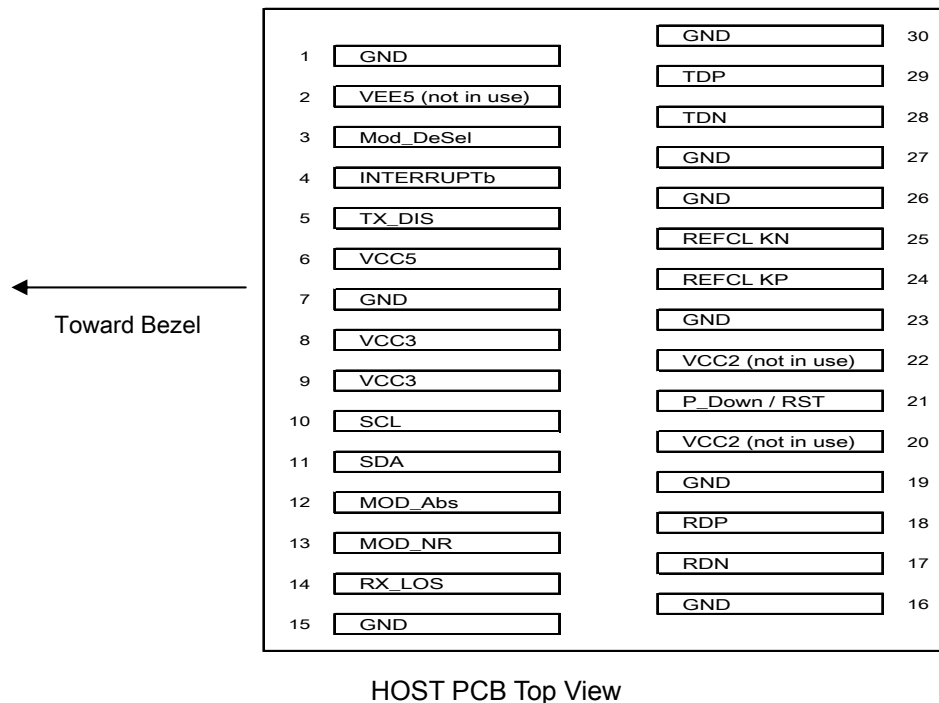


Figure 4.2. Host PCB XFP Pinout

4.3. Pin Descriptions

Table 4.3. Pin Description

Pin#	Name	Logic	Description	Note
1	GND		Module Ground	1
2	VEE5		-5.2V Power Supply; not in use	3
3	MOD_DeSel	LVTTL-I	Module De-select; When held Low allows module to respond to 2-wire serial interface	
4	INTERRUPTb	LVTTL-O	Indicates presence of an important condition, which can be read over the 2-wire serial interface. This pin is an open collector output and must be pulled up to host_Vcc on the host board.	2
5	TX_DIS	LVTTL-I	Transmitter Disable; When asserted High, transmitter output is turned off. This pin is pulled up to VCC3 in the module	
6	VCC5		+5V Power Supply	
7	GND		Module Ground	1
8	VCC3		+3.3V Power Supply	
9	VCC3		+3.3V Power Supply	
10	SCL	I/O	2-wire serial interface clock. Host shall use a pull-up resistor connected to host_Vcc of +3.3V.	2
11	SDA	I/O	2-wire serial interface data. Host shall use a pull-up resistor connected to host_Vcc of +3.3V.	2
12	MOD_Abs	LVTTL-O	Indicates Module is not present. Host shall pull up this pin, and grounded in the module. "High" when the XFP module is absent from a host board.	2
13	MOD_NR	LVTTL-O	Module not ready; When High, Indicates Module Operational Fault. This pin is an open collector and must be pulled to host_Vcc on the host board.	2
14	RX_LOS	LVTTL-O	Receiver Loss of Signal; When high, indicates insufficient optical input power to the module. This pin is an open collector and must be pulled to host_Vcc on the host board.	2
15	GND		Module Ground	

Pin#	Name	Logic	Description	Note
16	GND		Module Ground	
17	RDN	CML-O	Receiver Inverted Data Output; AC coupled inside the module.	
18	RDP	CML-O	Receiver Non-Inverted Data Output; AC coupled in side the module.	
19	GND		Module Ground	1
20	VCC2		+1.8V Power Supply; not in use	3
21	P_Down/RST	LVTTTL-I	Power down; When High, module is limited power mode. Low for normal operation. Reset; The falling edge indicates complete reset of the module. This pin is pulled up to VCC3 in the module.	
22	VCC2		+1.8V Power Supply; not in use	3
23	GND		Module Ground	1
24	REFCLKP	PECL-I	Reference clock Non-Inverted Input; not in use	
25	REFCLKN	PECL-I	Reference clock Inverted Input; not in use	
26	GND		Module Ground	1
27	GND		Module Ground	1
28	TDN	CML-I	Transmitter Inverted Data Input; AC coupled in side the module.	
29	TDP	CML-I	Transmitter Non-Inverted Data Input; AC coupled in side the module.	
30	GND		Module Ground	1

Note

- 1: Module ground pins are isolated from the module case and chassis ground within the module.
- 2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board.
- 3: Not connected internally.

5. Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	-5	85	degC	
Supply Voltage	VCC5	-0.3	6.0	V	
Supply Voltage	VCC3	-0.5	3.6	V	
Voltage on LVTTTL Input	Vilvttl	-0.5	VCC3+0.5	V	
LVTTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power(Average)	Mip	-	4	dBm	1

Note:

- 1: PIN Receiver

Table 5.2. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	-5	70	degC	1
		-5	85		2
Relative Humidity (non-condensing)	Rhop	-	85	%	
Power Supply Voltage	VCC5	4.75	5.25	V	
Power Supply Voltage	VCC3	3.135	3.465	V	
Power Supply Current	ICC5	-	500	mA	3
Power Supply Current	ICC3	-	750	mA	

Note:

- 1: SXP3100SV
2: SXP3100SV-M
3: The inrush current is included

6. Electrical Interface

6.1. High Speed Electrical Interface

XFI Application Reference model

Figure 6.1.1 shows the high speed electrical interface (XFI) compliance points.

XFI electrical interface is specified for each compliance point in the chapter 3 of the XFP MSA specification. Rev (4.0)

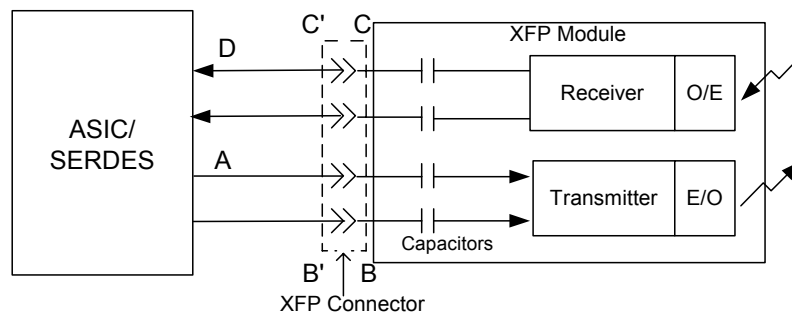


Figure 6.1.1. XFI Application Reference Model

XFI Module Transmitter Input Electrical Interface Specification at B'

Table 6.1.1. XFI Transmitter Input Electrical Specification at B'

Parameter -B'	symbol	Min	Typ	Max	Units	Note
Reference differential Input Impedance	Zd	-	100	-	Ohm	
Termination Mismatch	ΔZ_m	-		5	%	
Input AC Common mode Voltage		-		25	mV(RMS)	
Differential Input Return Loss	SDD11	20		-	dB	1
		8		-	dB	2
		See 3		-		3
Comon Mode Input Return Loss	SCC11	3		-	dB	4
Differential to Common Mode Conversion	SCD11	10		-	dB	4
Total Input Non-DDJ Jitter	TJtnd	-		0.41	UIp-p	
Total Input Jitter	TJ	-		0.61	UIp-p	
Input Jitter for ITU-T 20kHz-80MHz	Gjin1	-		150	mUIp-p	
Input Jitter for ITU-T 4MHz-80MHz	Gjin2	-		50	mUIp-p	
Eye Mask	X1	-		0.305	UI	5
	Y1	60		-	mV	
	Y2	-		410	mV	

Note

- 1: 0.05 to 0.1 GHz
- 2: 0.1 to 5.5GHz
- 3: 5.5 to 12GHz, $SDD11(dB)=8-20.66\log_{10}(f/5.5)$, with f in GHz
- 4: 0.1 to 15GHz
- 5: Eye Mask is defined in Figure 6.1.2

XFI Module Receiver Output Electrical Interface Specification at C'

Table 6.1.2. XFI Receiver Output Electrical Specification at C'

Parameter -C'	symbol	Min	Typ	Max	Units	Note
Reference differential Output Impedance	Zd	-	100	-	Ohm	
Termination Mismatch	ΔZ_m	-		5	%	
Output AC Common mode Voltage		-		15	mV(RMS)	
Output Rise and Fall time (20%-80%)	trh, tfh	24		-	ps	
Differential Output Return Loss	SDD22	20		-	dB	1
		8		-	dB	2
		See 3		-		3
Comon Mode Input Return Loss	SCC22	3		-	dB	4
Deterministic Jitter	TJtnd	-		0.18	Ulp-p	
Total Jitter	TJ	-		0.34	Ulp-p	
Eye Mask	X1	-		0.17	UI	5
	X2	-		0.42	UI	
	Y1	170		-	mV	
	Y2	-		425	mV	

Note

- 1: 0.05 to 0.1 GHz
- 2: 0.1 to 5.5GHz
- 3: 5.5 to 12GHz, $SDD11(dB)=8-20.66\log_{10}(f/5.5)$, with f in GHz
- 4: 0.1 to 15GHz
- 5: Eye Mask is defined in Figure 6.1.3

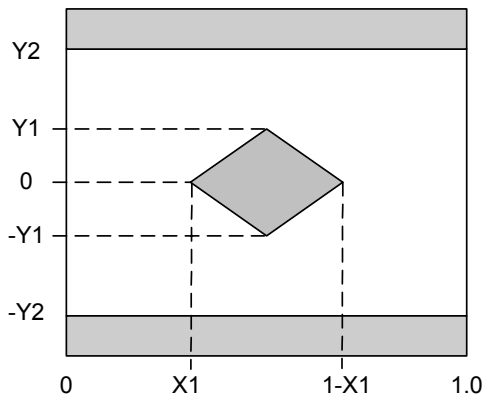


Figure 6.1.2.
Transmitter Input Eye Mask

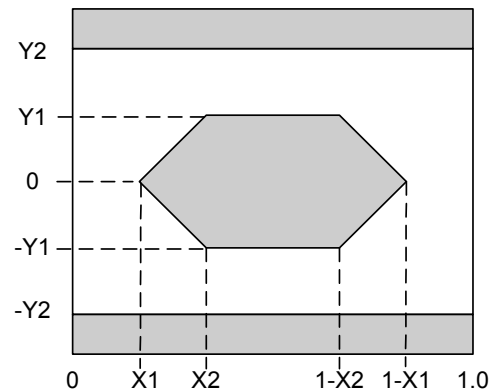


Figure 6.1.3.
Receiver Output Eye Mask

XFI Reference Clock Specification

Note that the reference clock is not needed for SXP3100SV-M. The differential reference clock signals if used are internally terminated across 100ohm as shown in Figure 2.1.

6.2. CDR Specification

Transmitter CDR

Table 6.2.1. Transmitter CDR Specification

Parameter	symbol	Min	Typ	Max	Units	Note
Jitter Transfer Bandwidth	BW	-		8	MHz	1
Jitter Transfer Peaking	Jp1	-		0.1	dB	2
	Jp2	-		1	dB	3

Note

- 1: In order to meet SONET/SDH jitter transfer requirement, de-jitter PLL will be needed on the host board SerDes.
- 2: Frequency \leq 120kHz
- 3: Frequency \geq 120kHz

Receiver CDR

Table 6.2.2. Receiver CDR Specification

Parameter	symbol	Min	Typ	Max	Units	Note
Jitter Transfer Bandwidth	BW	-		12	MHz	
Jitter Transfer Peaking	Jp1	-		0.1	dB	1
	Jp2	-		1	dB	2

Note

- 1: Frequency \leq 120kHz
- 2: Frequency \geq 120kHz

6.3. Low Speed Electrical Interface

Table 6.3.1. Low Speed Control and Alarm Signals Electrical Interface

Parameter	symbol	Min	Typ	Max	Units	Note
XFP Interrupt, Mod_NR, RX_LOS	V _{ol}	0.0		0.4	V	1
	V _{oh}	V _{cc} -0.5		V _{cc} +0.3		2
XFP TX_DIS, P_DOWN/RST	V _{il}	-0.3		0.8	V	3
	V _{ih}	2.0		V _{CC3} +0.3		4
XFP SCL and SDA Output	V _{ol}	0.0		0.4	V	1
	V _{oh}	V _{cc} -0.5		V _{cc} +0.3		2
XFP SCL and SDA Input	V _{il}	-0.3		V _{CC3} *0.3	V	5
	V _{ih}	V _{CC3} *0.7		V _{CC3} +0.5		6
Capacitance for XFP SCL and SDA I/O pin	C _i	-		14	pF	
Total bus capacitive load for SCL and SDA	C _b	-		100	pF	7
		-		400	pF	8

Note

- 1: Pull-up resistor must be connected to host_Vcc on the host board. I_{ol}(max)=3mA
- 2: Pull-up resistor must be connected to host_Vcc on the host board.
- 3: Pull-up resistor connected to V_{CC3} within XFP module. I_{il}(max)= -10μA.
- 4: Pull-up resistor connected to V_{CC3} within XFP module. I_{ih}(max)= 10μA.
- 5: Pull-up resistor must be connected to host_Vcc on the host board. I_{ol}(max)= -10μA.
- 6: Pull-up resistor must be connected to host_Vcc on the host board. I_{ol}(max)= 10μA.
- 7: at 400KHz, 3.0kohms, at 100kHz, 8.0kohms max.
- 8: at 400KHz, 0.8kohms, at 100kHz, 2.0kohms max.

7. Optical Interface

Table 7.1. Optical Interface

Transmitter Optical Interface						
Parameter	Symbol	Mn	Typical	Max	Unit	Note
Operating Data Rate	-	9.95		10.75	Gb/s	1
Output Center Wavelength	l _{tc}	1530		1565	nm	
Spectral Width	dl	-		1	nm	
SMSR	SMSR	30		-	dB	
Average Output Power	P _o	-1		2	dBm	2
Disabled Power	P _{off}	-		-30	dBm	2
Extinction Ratio	ER	8.2		-	dB	2
Optical Modulation Amplitude (10G Ethernet)	OMA	-1.7		-	dBm	3
Transmitter and dispersion penalty (10G Ethernet)	TDP	-		3	dB	3
OMA-TDP (10G Ethernet)	OMAtdp	-2.1		-	dBm	3
Eye Mask 1 (SONET/SDH)		GR-253-CORE/ITU-T G.691				2
Eye Mask 2 (10G Ethernet)		IEEE802.3ae				3
Generation Jitter 1 (20kHz - 80MHz)		-		0.15	Ulp-p	2, 4
Generation Jitter 2 (4MHz - 80MHz)		-		0.1	Ulp-p	2, 4
RIN ₂₁ OMA	RIN	-		-128	dB/Hz	
Optical Return Loss Tolerance		-		21	dB	
Receiver Optical Interface						
Parameter	Symbol	Mn	Typical	Max	Unit	Note
Operating Data Rate	-	9.95		10.75	Gb/s	1
Input Center Wavelength	l _{rc}	1260		1565	nm	
Overload	R _{ovl}	0.5		-	dBm	
Minimum Sensitivity	P _{min}	-		-14	dBm	2
Stressed Sensitivity in OMA	OMAst	-		-11.3	dBm	
RX_LOS Assert Level	RLOS _a	-30		-25	dBm	
RX_LOS Deassert Level	RLOS _d	-		-22	dBm	
RX_LOS Hysteresis	RLOS _h	1		5	dB	
Optical Return Loss	ORL	27		-	dB	
Jitter Tolerance	JTL	GR-253-CORE/ITU-T G.783				

Note:

- 1: Data rate tolerance
 IR-2/S-64.2b, 10GBASE-EW : typ.+/-20ppm
 10GBASE-ER : typ.+/-100ppm
- 2: Measured at 9.95328Gbps, Framed PRBS2³¹-1, NRZ
- 3: Measured at 10.3125Gbps, Non-framed PRBS2³¹-1, NRZ
- 4: Measured by using Sumitomo evaluation test board.

8. Electrical and Optical I/O Signal Relationship

Table.8.1. TX_DIS vs. Optical Output Power

TX_DIS	Optical Output Power
Low ($V_{IL} = -0.3$ to $0.8V$)	Enabled
High ($V_{IH} = 2.0$ to $VCC3+0.3V$)	Disabled ($< -30dBm$)

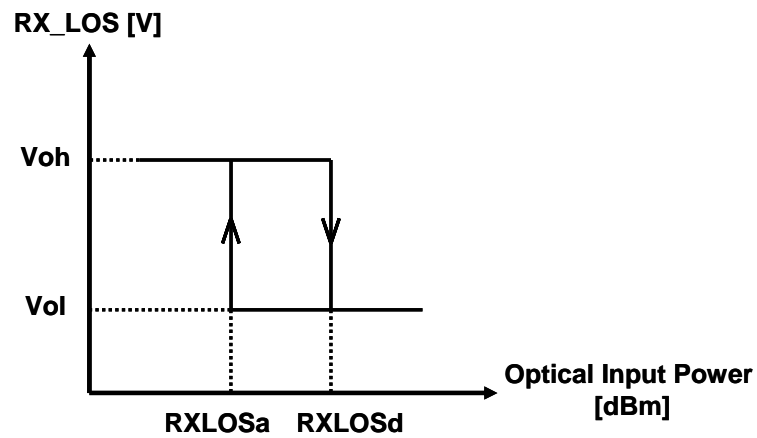


Figure.8.1. Optical Input Power vs. RX_LOS

9. User Interface

9.1. XFP Mechanical Interface

XFP Mechanical Interface is specified in the Chapter 6 in the XFP MSA specification.

XFP Mechanical Components

Figure 9.1 shows the XFP transceiver concept and mechanical components.

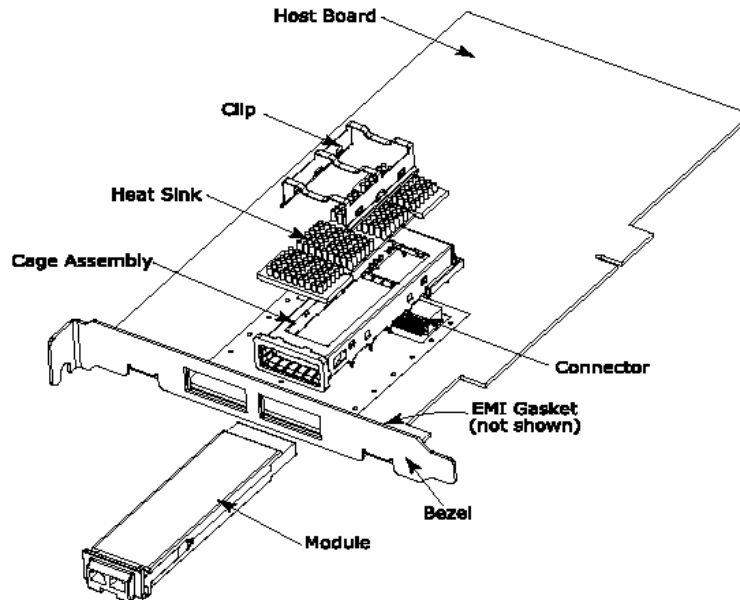


Figure 9.1. XFP Mechanical Interface Concept and Components

XFP Host board Mechanical Layout

XFP Host Board Layout is specified in the Figure 35 of the XFP MSA specification (Rev. 4.0).

Host Board XFP Connector Footprint and Layout

Host board XFP connector layout is specified in the Figure 36 of the XFP MSA Specification (Rev. 4.0).

XFP Datum Alignment and Bezel Design

XFP datum alignment (depth) is specified in the Figure 30 of the XFP MSA specification (Rev. 4.0).

The recommended bezel design is specified in the Figure 37 of the XFP MSA specification (Rev. 4.0).

XFP Connector and XFP Cage Assembly

The XFP 30-contact connector mechanical specification is shown in Figure 39 of the XFP MSA specification (Rev. 4.0)

The XFP Cage Assembly mechanical specification is shown in the Figure 41 of the XFP MSA specification (Rev. 4.0).

9.2. Management Interface

XFP 2-Wire Serial Interface Protocol

XFP 2-wire serial interface is specified in the Chapter 4 of the XFP MSA specification.

The XFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all XFP modules.

The 2-wire serial interface address of the XFP module is 1010000X(A0h). In order to access to multiple modules on the same 2-wire serial bus, the XFP has a MOD_DESEL (module deselect pin). This pin (which is pull high or deselected in the module) must be held low by the host to select of interest and allow communication over 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

XFP Management Interface

XFP Managed interface is specified in the Chapter 5 of the XFP MSA specification.

The Figure 9.2 shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is always directly available and is used for the diagnostics and control functions that must be accessed repeatedly. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

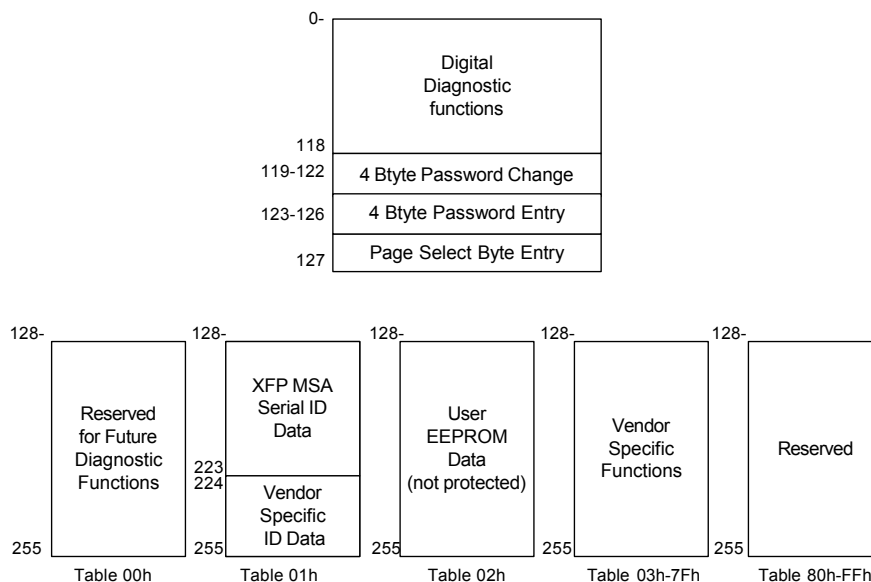


Figure 9.2. 2-wire Serial Interface Memory Map

9.3. A/D Accuracy and Values

Table 9.3.1. A/D Values

Byte	Bit	Name	Description
96	All	Temperature MSB	Signed 2's complement integer temperature (-40 to +125degC) based on internal temperature measurement
97	All	Temperature LSB	Fractional part of temperature(count/256)
98-99	All		Reserved
100	All	Tx Bias MSB	Measured Laser Bias Current in mA. Bias current is full 16 bit value *2μA. (Full range of 0 to 131mA)
101	All	Tx Bias LSB	
102	All	Tx Power MSB	Measured Tx output power in mW. Tx power is full 16 bit value *0.1μW. (Full range of -40 to +8.2dBm)
103	All	Tx Power LSB	
104	All	Rx Power MSB	Measured Rx input power in mW. Tx power is full 16 bit value *0.1μW. (Full range of -40 to +8.2dBm)
105	All	Rx Power LSB	
106	All	Vcc MSB	Internally measured transceiver supply voltage. Vcc is full 16 bit value*100μV. (Full range of 0 to +6.55 Volts)
107	All	Vcc LSB	
108	All	AUX 2 MSB	TBD
109	All	AUX 2 LSB	

Table 9.3.2. A/D Accuracy

Data Address	Parameter	Accuracy	Relative accuracy	Units Display	Note
96-97	Temperature	+/-3degC	NA	Signed 2's complement integer degC	Junction temperature of monitoring IC.
98-99	Reserved				
100-101	Tx Bias	+/-10%	NA	×2μA	Specified by nominal value
102-103	Tx Power	+/-2dB@BOL (Note1) (Range: -1 to +2dBm)	+/-1dB (Note2)	×0.1μW	Average Power
104-105	Rx Power	+/-2dB@BOL (Note1) (Range: -16 to +2dBm)	+/-1dB (Note2)	×0.1μW	At specified transmitter wavelength.
106-107	Vcc	+/-3%	NA	×100μV	+3.3V Only

Note

- 1: Over specified temperature and voltage.
- 2: Over specified temperature and voltage range over the life of the product into a fixed measurement system.

9.4. Serial ID Memory Map (Data Field – Page 01h)

Address	Size (Bytes)	Name	Hex	ASC	Description
Base ID Field					
128	1	Identifier	08		XFP module
129	1	Ext. Identifier	90		3.5W Max
					With CDR
130	1	Connector	07		LC Connector
131	8	Tranciver	22		10GBASE-ER/EW
132			00		
133			00		
134			00		
135			00		
136			20		S-64.2b
137			00		
138			00		
139	1	Encoding	B0		64B/66B, SONET Scrambled, NRZ
140	1	BR-Min	64		9.95Gbps
141	1	BR-Max	6C		10.75Gbps
142	1	Length (SMF)-km	28		40km
143	1	Length (E-50 μm)	00		
144	1	Length (50 μm)	00		
145	1	Length (62.5 μm)	00		
146	1	Length (Copper)	00		
147	1	Device Tech	74		1550nm EML, PIN Detector
148	16	Vendor name	53	S	
149			75	u	
150			6D	m	
151			69	i	
152			74	t	
153			6F	o	
154			6D	m	
155			6F	o	
156			45	E	
157			6C	i	
158			65	e	
159			63	c	
160			74	t	
161			72	r	
162			69	i	
163			63	c	
164	1	CDR Support	F0		
165	3	Vendor OUI	00		
166			00		
167			5F		
168	16	Vendor PN	53	S	
169			58	X	
170			50	P	
171			33	3	
172			31	1	
173			30	0	
174			30	0	
175			53	S	
176			56	V	
177			20/2D	/-	
178			20/4D	/M	
179			20		
180			20		
181			20		
182			20		
183			20		
184	2	Vendor rev	41 to 5A	A to Z	
185			20		
186			79		
187	2	Wavelength	18		1550nm @ RT
188			0F		
189	2	Wavelength Tolerance	A0		+/-20nm (Note1)
190	1	Max Case Temp	40/55		70degC/85degC
191	1	CC_BASE	Note2		
Extended ID Field					
192	4	Power Supply	AF		3.5W
193			96		1.5W (Note3)
194			A8		500mA/800mA @ +5.0V/+3.3V
195			00		(Note4)
196	16	Vendor SN	Note5		
197					
198					
199					
200					
201					
202					
203					
204					
205					
206					
207					
208					
209					
210					
211					
212	8	Date Code & Lot Code	Note6		Year
213					Month
214					Day
215					Lot
216					
217					
218					
219					
220	1	Diagnostic Monitoring Type	08		No BER Support
					Average Power
221	1	Enhanced Options	60		Optional Soft TX Disable
222	1	Aux Monitoring	70		Optional Soft P down
223	1	CC_EXT	Note7		+3.3V Support Voltage
Vendor Specific ID Fields					
224	32	Vendor Specific			
225					
226					
227					
228					
229					
230					
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232					
233					
234					
235					
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237					
238					
239					
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255					

Note

- 1: The guaranteed +/- range of transmitter output wavelength under all normal operating conditions.
- 2: Address 191 is check sum of bytes 128 to 190.
- 3: Maximum total power dissipation in power down mode.
- 4: +1.8V/-5.2V is not in use.
- 5: Address 196 to 211 Vendor Serial Number Note6. Address 212 to 219 Date code
- 7: Address 223 is check sum of bytes 192 to 222.

9.5. Supply filter

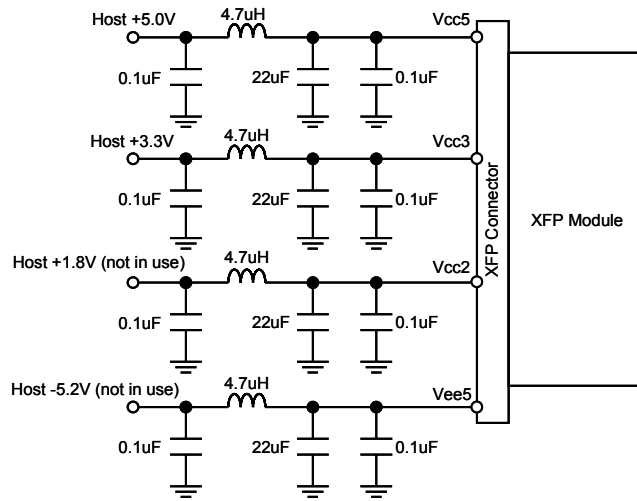


Figure 9.5. Supply Filter

9.6. Recommended Electrical Interface

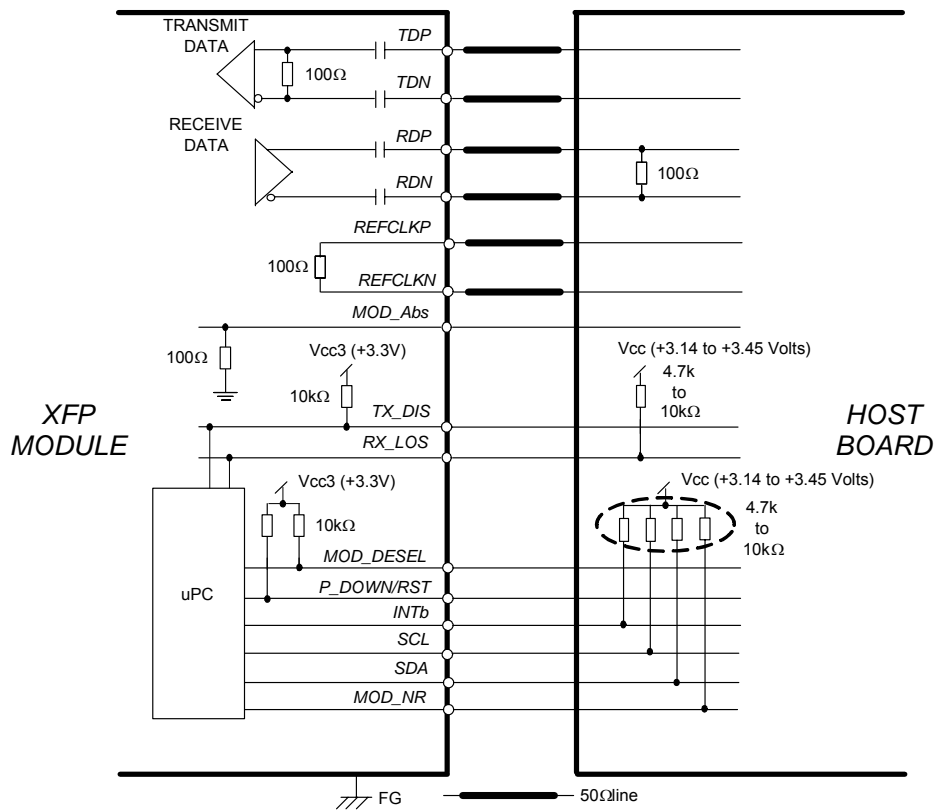


Figure 9.6. Recommended Electrical Interface

10. Qualification Testing

SXP3100SV-M 10Gb/s transceiver is qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

11. Laser Safety Information

SXP3100SV-M OC-192 transceiver uses a semiconductor laser system that is classified as Class 1 laser products per the Laser Safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC 60825-1:2001 International standards.

Caution

If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

12. Electromagnetic Compatibility (Pending)

EMI (Emission)

SXP3100SV-M is designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

RF Immunity

SXP3100SV-M has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

Electrostatic Discharge (ESD) Immunity

SXP3100SV-M has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

14.5. I2C Interface

If the serial clock(SCL) is more than 100kHz, the SCL is held in line low(clock stretching) during an I2C read or write operation.

15. Contact Information

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